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Implementation of Discrete Wavelet Transform for Image Compression Using Enhanced Half Ripple Carry Adder

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ABSTRACT

The aim is to design an efficient two-dimensional Discrete Wavelet Transformation (DWT) based image compression technique. In order to achieve best performance, Enhanced Half-Ripple Carry Adder (EHRCA) has been designed. Verilog Hardware Description Language (Verilog HDL) is used to model the EHRCA and DWT technique. DWT technique has been designed with the help of two types of filtering technique known as Low Pass Filter (LPF) and High Pass Filter (HPF). Three levels of decomposition are made by DWT process and each process has two levels compressions called "Row Wise Compression" and "Column Wise Compression". In proposed DWT models, adders are recognized as high potential than other components. In order to improve the efficiency of DWT process, an efficient adder called "Enhanced Half-Ripple Carry Adder (EHRCA)" has been designed in this research work. Proposed EHRCA circuit offers 10.71% improvements in hardware slice utilization, 11.78% improvements in total power consumption than traditional Binary to Excess 1 Conversion (BEC) based Square Root Carry Select Adder (SQRT CSLA). Further proposed adder has been incorporated into Row Wise Compression and Column Wise Compression for improving the architectural performances of DWT. In future, proposed EHRCA based DWT will be useful in Discrete Cosine Transformation (DCT) and hybrid type and lifting based DWT techniques.

Keywords:Discrete Cosine Transformation (DCT),Enhanced Half-Ripple Carry Adder (EHRCA),Binary to Excess Conversion (BEC),Square Root Carry Select Adder (SQRT CSLA).

INTRODUCTION

The adders of the digital circuits and wavelet transformations play a vital role.The work is developed with the help of adders in order to develop the enhanced half ripple carry adder[1].The wavelet transformation is used in order to perform the compression.In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic units, but also in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations[2,3].Although adders can be constructed for many numerical representations, such as binary-coded decimal or excess-3, the most common adders operate on binarynumbers. In cases where two's complement or ones' complement is being used to represent negative numbers, it is trivial to modify an adder into an adder–subtractor. Other signed number representations require more logic around the basic adder.The half adder adds two single binary digits *A* and *B*. It has two outputs, sum (*S*) and carry (*C*). The carry signal represents an overflow into the next digit of a multi-digit addition. The value of the sum is $2C + S$. The simplest half-adder design, pictured on the right, incorporates an XOR gate for *S* and an AND gate for *C*. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder.Discrete Wavelet Transformation (DWT) is the technique for decomposing/compressing the images[4]. Also DWT represents as an image which is the sum of wavelet functions (wavelets) with different location and scale. It represents the data into a set of low pass and high pass coefficients. The input data is passed through set of low pass and high pass filters. The output from high pass filters and low pass filters are down sampled by 2. The output from low pass filter is an average coefficient and the output from high pass filter is a detail coefficient. In 2-D DWT, the input data is passed through set of both low pass and high pass filter in two directions, both rows and columns. As in 1-D DWT, the outputs from low pass and high pass filters are down sampled by 2 in each direction. In coefficient representation, the first alphabet represents the transform in row whereas the second alphabet represents transform in column. The representation L means low pass signal and H means high pass signal. Three levels of decomposition are done to compress the image with the help of EHRCA. Similarly, in reconstruction, input data can be achieved in multiple resolutions by decomposing the

LL coefficient further for different levels. The compressed data is up-sampled by a factor of 2 in order to reconstruct the original input data while performing interpolation process [5,6,7].

PROPOSED SYSTEM-Enhanced Half Ripple Carry Adder

It is possible to create a logical circuit using multiple full adders to add *N*-bit numbers. Each full adder inputs a C_{in}, which is the C_{out} of the previous adder. This kind of adder is called a ripple-carry adder, since each carry bit "ripples" to the next full adder. Note that the first (and only the first) full adder may be replaced by a half adder (under the assumption that $C_{in} = 0$).

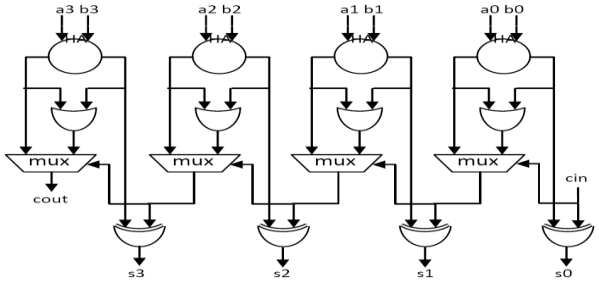


Fig 1.Circuit diagram for 4-bit EHRCA circuit

The layout of a ripple-carry adder is simple, which allows for fast design time; however, the ripple-carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit. Each full adder requires three levels of logic. In a 32-bit ripple-carry adder, there are 32 full adders, so the critical path (worst case) delay is 3 (from input to carry in first adder) + 31 * 2 (for carry propagation in later adders) = 65 gate delays. The general equation for the worst-case delay for a *n*-bit carry-ripple adder is

$$T_{CRA}(n) = T_{HA} + (n-1)\cdot T_c + T_s = T_{FA} + (n-1)\cdot T_c = 6D + (n-1)\cdot 2D = (n+2)\cdot 2D \quad \text{---------- (1)}$$

The delay from bit position 0 to the carry-out is a little different:

$$T_{CRA_{[0:c_{out}]}} = T_{HA} + n \cdot T_c = 3D + n \cdot 2D \quad \text{----------(2)}$$

The carry-in must travel through *n* carry-generator blocks to have an effect on the carry-out

$$T_{CRA_{[c0:cn]}}(n) = n \cdot T_c = n \cdot 2D \quad \text{----------(3)}$$

A design with alternating carry polarities and optimized AND-OR-Invert gates can be about twice as fast.RCA is one of the basic adders to perform the binary addition process. However, CPD is the main disadvantages in RCA circuit (i.e.,) every stage must have wait for carry signal from previous stage. In order to reduce the problem of CPD in RCA circuit, Enhanced Half Ripple Carry Adder (EHRCA) is developed.The circuit diagram for developed EHRCA circuit for 4-bit is illustrated in Figure 1. It consists of HAs, OR gate, AND gate and Multiplexors for performing addition process. As the name itself, final half of the circuit only (Multiplexors part) must have to wait until carry signal load from previous stage, remaining circuits can execute in a parallel manner. Hence, this adder circuit named as Enhanced Half Ripple Carry Adder. In other hand, the structure of this circuit is like that SQRT CSLA. Instead of RCA-BEC combination for Cin = 0 and Cin = 1 respectively of CSLA circuit, simplified circuit is designed as shown in Figure 1. The carry input is considered only final stage of EHRCA whereas remaining circuit can perform the respective computation in a parallel manner with the help of available input data. The EHRCA circuit for 8-bit and 16-bit can be designed. Further, the EHRCA adder is incorporated into the addition process of

Equation (3) to increase the performance of 2-D DWT. Three levels of decomposition are made for image compression. The performances of conventional SQRT CSLA and developed EHRCA circuits are analyzed in Results and Discussion.

EXPERIMENTAL RESULTS

The input image is shown in the figure 2.The simulation result for 2-D DWT compression are shown.The Level-1 compressions is shown in figure 8, Level-2 compressions is shown in figure 9 and Level-3 compressions is shown in figure 10.The input image is converted into the pixels and these pixels are demonstrated in Figure 2. Three levels of decomposition are made in this for image compression with the help of DWT and EHRCA. The input image to determine the DWT coefficients is shown in Figure 2. Three levels of decomposed images are illustrated in the figure 3-6 respectively.The overall MATLAB results are shown in figure 7. The images have multi-resolution decomposition capability. Three levels of decomposition are done to compress the image with the help of EHRCA. In reconstruction, input data can be achieved in multiple resolutions by decomposing the LL coefficient further for different levels. The compressed data is up-sampled by a factor of 2 in order to reconstruct the original input data while performing interpolation process

Fig 2.Input image Fig 3.Row wise compression

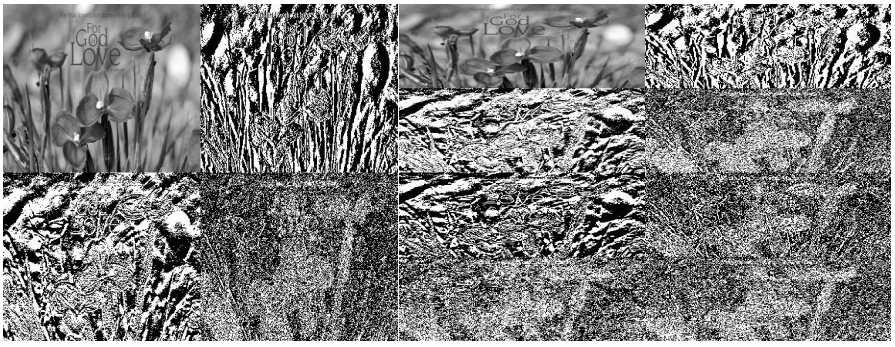
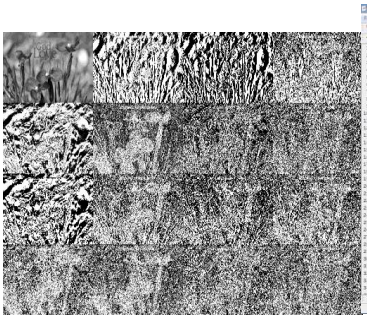


Fig 4.DWT LEVEL-1 compression Fig 5.DWT LEVEL-2 compression



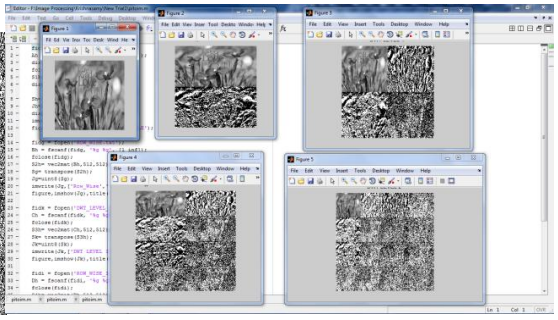
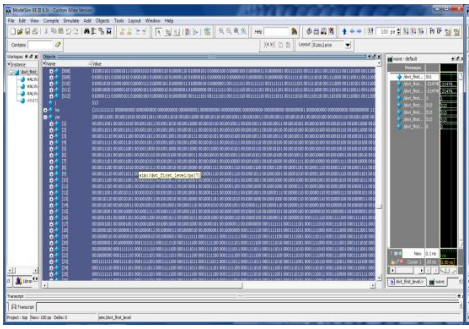


Fig 6.DWT LEVEL-3 compression Fig 7.Overall DWT compression outputs



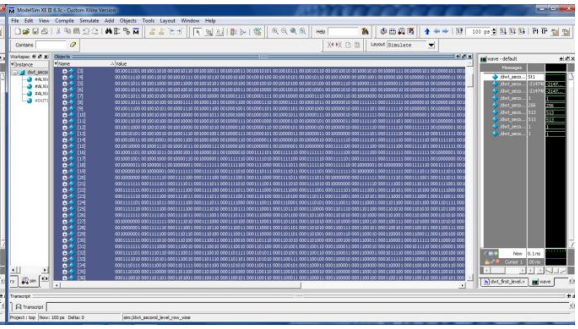


Fig 8.DWT LEVEL-1 compressionFig 9.DWT LEVEL-2 compression

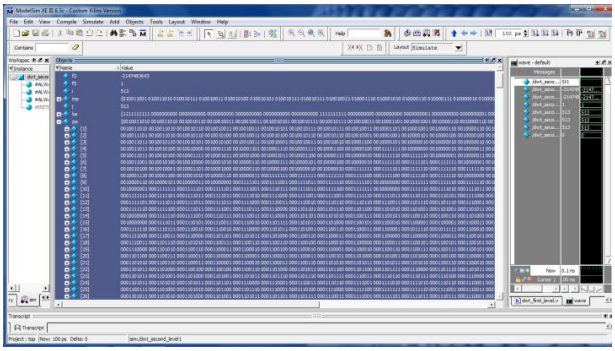


Fig 10.DWT LEVEL-3 compression

Enhanced Half Ripple Carry Adder (EHRCA) circuit is designed using Verilog Hardware Description Language (Verilog HDL). The validation of proposed adder circuit is evaluated using Model Sim 6.3C and Synthesis results are evaluated by using Xilinx 10.1i design tool. Also levels of decomposition of image using 2-D DWT are measured using MATLAB tool. The RCA circuit is realized and identified the redundant logic operations. Based on identified redundant logic, EHRCA circuit is designed.The circuit of EHRCA is most likely conventional BEC based SQRT CSLA. Hence, the performance of conventional BEC based SQRT CSLA and developed EHRCA circuit for 16-bit is compared in Table 1.

Table1. Comparison of 16-bit conventional BEC based SQRT CSLA and developed 16-bit EHRCA circuits

TYPE	slices	LUT	delay(ns)	power(mW)
16-bit Conventional BEC based SQRT CSLA	28	47	15.971	280
16-bit developed EHRCA	25	42	16.707	247

From Table 1, it is clear that 16-bit developed EHRCA circuit offers 10.71% reduction in silicon area and 11.78% reduction in power consumption than conventional BEC based SQRT CSLA. Therefore, developed EHRCA circuit is the best choice for 2-D DWT implementation. Further, the developed EHRCA circuit is incorporated into 2-D DWT addition process to improve the performance.

CONCLUSION

The 2-D DWT based image compression is developed with the help of Enhanced Half Ripple Carry Adder (EHRCA). The design of EHRCA and incorporation of EHRCA into DWT computation is done by Verilog HDL. The developed EHRCA circuit consumes less hardware resources and power consumption than conventional BEC based SQRT CSLA. The developed EHRCA circuit offers 10.71% reduction in silicon area and 11.78% reduction in power consumption than conventional BEC based SQRT CSLA. Further, developed EHRCA circuit is incorporated into addition process of 2D-DWT for image compression. Three levels of decomposition are made . Simulation results for image compression using 2-D DWT is validated by both Model Sim 6.3C and MATLAB simulation tools. In future, the developed EHRCA based 2-D DWT will be helpful for image processing applications like compression, segmentation and fragmentations.

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