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SURVEY ON VLSI BASED DESIGN FOR IMAGE SUPER RESOLUTION AND RESTORATION

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Abstract

High Resolution Images (HRI) are needed and is often required in most of the electronic imaging applications. In order to execute such real time applications ex. machine inspection, object detection, missing car plate reorganization CMOS based VLSI Designs are used. In general VLSI based image processor chip includes the coordinate accumulator, line buffer, weighting coefficient generator; vertical interpolator, horizontal interpolator and each of the units perform specified operations. VLSI based image sensor is required to get input image from external environment and is processed on VLSI architecture such as either Field Programmable Gate Arrays (FPGA) or Application Specific Integrated Circuit (ASIC). FPGAs are best choice for the VLSI designer to check the functionality and synthesize and implemented the design. In image processing FPGAs are required for implementing various image processing algorithms such as motion detection, image enhancement, and image de noising and image compression. In this paper we will describe some of the advanced works and the methodology to design VLSI based digital image processor for reducing noise, enhancing the resolution and restores the original image from set of noisy images. Also, investigated the super resolution algorithms, their limitations and future scope is also presented.

Keywords- Image de noising, VLSI FPGA, Parallel Processor, Super resolution, pipelining.

I. INTRODUCTION

High Resolution images are having more importance than low resolution images since it has more information [1].However, these HR images requires more memory to store, more time is required to process it but it will be helpful in order to monitor the industry automation, aerial survey, patient health monitoring etc. For example, HR medical images are very helpful for a doctor to make a correct diagnosis. Up to 1970's, charge couple device (CCD) and complementary metal oxide semiconductor (CMOS) based sensor technology was used to get the images from the scene. Later as the technology go on increasing the device size and price is to be reducing and peoples wants less complex, user friendly and more compatible devices preferred. Hence, it is toughest task for the VLSI designers to meet such expectations. In early period image processing has been used in many applications such as in radar imaging, satellite imaging [2] etc.

During that time image filtering and image recondition were developed and the processing systems were big and of high cost also the number of users were small. After imaging technologies were implemented in medical field such MRI, CT, PET and used in entertainment industries [3]. Now days due to enriched technologies digital cameras, iPods, high-definition televisions etc. have become personal. The availabity of these products in our hand is due to the result of advanced research and developments in algorithms and theory as well as in the areas of system architectures and very large scale integrated circuit designs with low manufacturing cost, small chip size and low power consumption. Submicron, Nano technology the efficient circuit design such as pipeline architecture and parallel processing propelled VLSI to its peak. Research in image processing problems facing continuous challenges by new technology enhancements and different coding algorithms. This has motivated us to develop such a VLSI based image processing systems with low cost and low power consumption while enhancing the clarity and reducing the noises of the image. From past two decades many researchers works on super resolution reconstruction algorithms [4]. The major advantage of super resolution approaches is that it takes less cost and less expensive, since the available LR frames are utilized [4]. Different algorithms works on LR frames to produce required HR image.

A. FPGA for Image processing

Initially FPGAs are permitted only for interconnection later technology improves and more no. of circuit components are available i.e. device density improves. Hence it is used an almost all applications like image processing, signal processing, implementation of communication networks and medical imaging [5] etc.Figure.1 gives you the typical VLSI design flow, as compared to ASIC (application specific integrated circuit) FPGAs have more features and it is user friendly. Table1. Gives difference between FPGA and ASIC technologies. The main aim of any VLSI based design is to take less power to finish the scheduled task in a less time; the complexity should be decreases as it results reducing the chip size. By keeping all these parameters the device practitioner or designer take suitable methodology, optimization algorithms has to be selected according to given applications. After designing, its functionality is verifying, corresponding RTL

code is synthesized, programmed into an FPGA device and verifying the post simulation. Basically FPGA consists of programming elements (PEs) called LUTs (Xilinx).

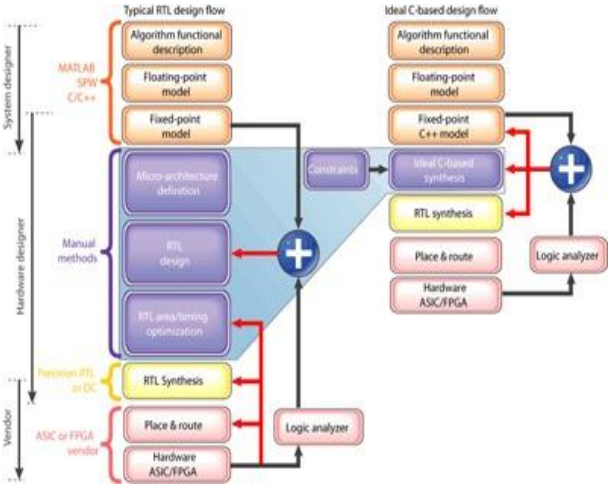

Fig. 1. Typical VLSI Design flow

In addition to that, using different tools to make more optimized design and verifying the floor plan i.e. partitioning the circuits elements accordingly in required area, after verifying the place and route (by making more optimized) , post timing report. If it meets given specifications the final net list called GDS-II file generates corresponding chip.

TABLE I: SOC TRADE-OFFS.

Technology	Performance	Area	Program	power	Time
ASIC	High	Low	Low	Low	high
FPGA	Medium	High	High	High	Medium
Multiprocesr	High	High	High	High	Medium
DSP	Low	Medim	High	Medium	Low
DSP+coproc	High	High	High	Medim	medim

B. Concept of Super resolution

Due to less illumination conditions, improper sensor resolution, movement of either object or acquisition device high resolution frame gets distorted. Fig 2. Will gives how to make SR image from set of LR images taken by low resolution sensor. Super resolution problem can be modeled as Y= DBMKX + N, here B is Blur matrix D is down sampling operator, X is original HR image and N is the noise. To improve the spatial resolution of the image we often use: increase the No.of pixels or to make more pixels, if we decrease the pixels size shot noise will coming to existence. Another approach is increase the size of the chip but it will create delay problem since more capacitance more time to charge. The last one is increasing the resolution of the sensor will increases the sensor cost [1]. The high cost for high precision optics and image sensors is also an important concern in many commercial applications regarding HR imaging. Therefore, a new approach toward increasing spatial resolution is required to overcome these limitations of the sensors and optics manufacturing technology.

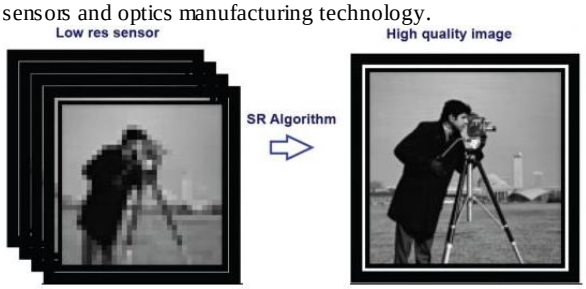

Fig 2. Concept of super resolution (from LR images to HR image)

The process of converting from low resolution images (frames) into high resolution image is called super resolution. Now the question arises why we need convert? As mentioned in earlier that these low resolution images(low frequency) consists less information and less number of pixels, with the help of this type of images not possible to identify exact information that are stored in LR images since noise is dominating. Medical imaging, astronomy applications, forensic, consumer and industrial automation applications used images regularly to perform given task. Therefore, by using this images couldn't give satisfactory results, hence we need to enhance the quality of the image. Basically super resolution methods are spatial domain and frequency domain. In frequency domain methods, using different transforms like discrete cosine transform (DCT) and discrete wavelet transform (DWT) the LR image is transformed into HR image, but these are expensive and it can't provide expected results .Later these methods are dominated by spatial domain, in this type of methods interpolation operations are performed directly on pixels(picture elements). From the past two decades lot of papers demonstrated different algorithms some of them are used for motion estimation, image de noising, de blurring, image restoration etc. The organization of the paper as follows part I describes the introduction on super resolution and FPGA for implementation, various state of the methods and their limitations are mentioned in part II, the motivation behind this work is presented in part III, finally conclusion and future scope is discussed in part IV.

II. RELATED WORKS

A novel super resolution algorithm based on irregular sampling (SRIS) proposed by Maria Pantoja,et.al.[5] here the high resolution (HR) frame was obtained by interpolating one or more previous frame and the resulted interpolated frame had samples with non-uniformly spaced areas. Their SRIS algorithm for reconstruct the image had the following process. They are implemented 3-D recursive method to obtain true motion vectors between low resolution frames. After that creates an interpolated frame with current and previous frames, thus obtained irregular sample patterns of the objects that were in motion. Finally they had reconstructed a higher resolution using Allebach algorithm with varonai implementation. Their proposed solution was not targeted any specific application but they had specifically tested the algorithm in a transcoded environment and experimental

results showed that their proposed algorithm improve quality significantly.

E. Quevedo, et.al. [6] had presented a selective filter to decide the best low resolution (LR) frame to be used in the super – resolution process . In addition to this they had divided each frame into macro-blocks (MBs) and analyzed each macro-block independently for better performance. For this they had implemented baseline super-resolution (BSR) algorithm which had few stages. In their first stage window selective filter (WSF) was used which contain the temporarily adjacent frame to the current frame. Their second stage was known as motion estimation which was the process of motion vectors determination that describes the transformations of pixels in space. The main absolute difference (MAD) between frames was also calculated by them, for micro blocks size deduction and a block selective filter was used for macro blocks selection. Their final stage was called fill holes in this each empty pixel were filled by a bilinear surface interpolator. Their results were provided in a test environment to objectively compare the image quality enhancement obtained by their proposed work with bilinear interpolation, and the baseline SR algorithm, also they had presented a quantitative comparison based on peak signal to noise ratio (PSNR) and structural similarity Index (SSIM) parameters. Finally they stated that their proposed algorithm significantly speeds up the previous one, it allow real time execution under certain conditions.

A novel adaptive detection tree based de-noising method (DTBDM) and its VLSI structure for random valued impulse noise removal is presented by Chih-Yuan Lien, et.al [7].The noise considered in their research was random valued impulse noise. They adopt a 3X3 mask for image denoising and DTBDM consists of two components decision tree based impulse detector and edge preserving image filter. They had employed a decision tree based impulse detector and edge preservation filter which can be realized easily with VLSI circuits was adapted by them. The architecture consists of line buffer and register bank to produce an output at every clock cycle was implemented. The VLSI architecture of their design yield a processing rate of 200MHz by using TMC 0.18 m technology. The advantage of their design was that it required only low computational complexity and two line memory buffers and its hardware cost was low and suitable to be applied to many real time applications.

A.Bhaskar Rao, et.al [8] had proposed a super resolution using sparsity their main focus was on the problem of improve the super resolution version of a given low resolution image. They adopted two constraints to resolve image reconstruction problem they are: the recovered image should be consistent with input image. Sparse Representation in prior assumes that the high resolution patches can be sparsely represented in dictionary. This model can successfully applied for reducing artifacts. They created dictionaries from simple random sampled raw patches from trained images of similar statistical nature using sparse coded algorithm. They implemented work in dot net for enhancing generic images such as flowers, human faces . Then two dictionaries for high resolution and low resolution image patches were trained using patch pairs. Experimental results demonstrated effectiveness of the sparsity as a prior for patch based super resolution for images.

Pulak Mondal, et.al [9] had proposed a parallel pipelined architecture with Affine Transform pixel representation (ATPR) algorithm. In their proposed system ATPR algorithm was able to calculate transform of only 2 pixels located in parallel. Later modified ATPR called MATPR by exploiting the replication nature of the pixel locations, but MATPR algorithm proposed by then was capable of transform calculation of a novel location from a single transform operation. This will accelerate the transform process and reduce the processing time of medical image registration. Their architecture was mapped in FPGA for prototyping and verification.

Jianchao Yang, et.al. [10] had presented a novel approach to solve single image super resolution problem with the help of image patches. Sparse representation of LR image means taking single atom from a complete dictionary. In this approach first construct dictionary from a pre trained images of low and high resolution images. Creation of dictionary will decide the efficiency of the reconstructed algorithm. Normally dictionary size gives the reconstruction error. If LR image details are not sufficient to construct the dictionary first use pre processing with bi-cubic interpolation. Their model was simultaneously applied for enhancing the resolution and face hallucination. The problem with this approach is construction of dictionary is complex task. Huimin Yao, et.al [11] had presented the complete VLSI based system on a chip (SOC) for high resolution depth sensing based on active infrared structured light which is going to be estimate the depth of 3D scene by enhancing consistency of speckle patterns. Their proposed system was a simple and efficient hardware structure for a block-matching based display estimation algorithm. Which facilitate rapid generation of clarity images in real time. Also they had designed a hardware friendly solution crated a look up table from a curve fitted calculate and calibrate the depth value in single step which does not to explicitly calibrated the parameter of the image sensors. Such as the length of the baseline. They had implemented their idea on system on chip (SOC) using FPGA. kenta takagi, et.al. [12] Proposed a real- time object detection system using Histogram Oriented Gradients (HOG) feature extraction VLSI accelerator. Their proposed work involves three techniques: first, VLSI oriented HOG algorithm with early classification in Super Vector Machine (SVM) classification, second , a dual core architecture for parallel feature extraction and a detection window-size scalable architecture with a reconfigurable MAC array for processing objects of different shapes a Multi object detection system and multiple scale object detection system were implemented by them to demonstrate the system flexibility and scalability of VLSI and applicability for versatile application in object detection. Their test chip was fabricated using 65nm CMOS technology.

Haibing Yin,et.al.[13] had presented a methodology by combined global hierarchical search and local full search and proposed a hardware efficient Integer Pixel Motion Estimation (IME) algorithm VLSI architecture with optimized on chip buffer structure . Their major contribution of work was improve hierarchical of IME Algorithm, multistage on-chip reference pixel buffer structure with high data reuse

between integer, fraction pixel motion estimation and highly reused and reconfigurable processing element structure. Their combo design of efficient algorithm and architecture was supposed to trade-off multiple target parameter including throughput capacity, local gate, on-chip standard RAM size, memory bandwidth, and on chip buffer structure were crucial factors for IME architecture design, accountable for multiple target performance trade-off. Kaulgud and Desai [14] discuss the use of wavelets for zooming images. Although zooming of a single image does not strictly fall in the realm of super-resolution, it is nevertheless interesting to study zooming from a wavelet perspective in order to seek pointers towards use of wavelets for SR problem. The authors use a multi-resolution analysis based on zero trees to estimate the wavelet coefficients at a finer scale after which inverse wavelet transform is taken to obtain the zoomed image. They extend this method to color images where the K-L transform is used to generate the (monochrome) principal component of the color image which is then zoomed using the multi-resolution technique.

Rajan and Chaudhuri [15] develop a method called generalized interpolation and use it to generate super-resolution images. In generalized interpolation, the space containing the original function is decomposed into appropriate subspaces such that the rescaling operation on individual subspaces preserves the properties of the original function. The combined rescaled sub-functions lead us back to the original space containing the interpolated function, possibly with less information loss compared to direct interpolation in the original space. This method is shown to be effective in structurepreserving super-resolution and in super-resolution rendering. In addition, the generalized interpolation is applied to perceptually organized image interpolation and to transparency.

Komatsu, Aizawa[16] and Saito address the problem of increasing the spatial resolution using multiple cameras with different apertures. The motivation for using multiple apertures stems from the fact that the spatial uniformity in the generated high resolution image in the case of same apertures is guaranteed if and only if multiple cameras are coplanar and the object of imaging is a two-dimensional plate perpendicular to their optical axes. Their super-resolution algorithm consists of an iterative two stage process of registration and reconstruction from non-uniformly spaced samples and is based on the Landweber algorithm.

Ching Wei Tsengal et.al [17]. Super resolution depth image concept was proposed. In this approach several RGB-D images are taken from scene with different directions and to aligned together to get depth image. But due to RGB-D sensor more noise as well as blurriness is introduced in depth images. Hence in order to reduce the noise and blurriness they performing some refinement steps through guided filtering and the results are combined with SRCNN learning method to get high resolution depth image . Dong et.al[18]. Presented single image super resolution with convolution network (SRCNN), this approach will give best results, but it performs badly in some situations is that this algorithm will sharpen the high frequency details in the image even when the misalignment is happen, it leads to jagged edge problem so in order to overcome this problem guided image up scaling is needed for smoothing. Jiwon Kim[19] writes in his paper SRCNN suffers from three problems such as, it works only for limited images, more time to convergence and network works only for single scale. In order to solve these issues jiwon Kim [3] extends Dongs work i.e. SRCNN with residual learning and gradual clipping for multi scale single network. Large deep (image depth) will produce better results. The amount of time it takes to convergence is low since more learning rate than conventional neural network. Authors also showed that if we increase the depth more and more it will gives better results. Finally this algorithm can also use for image restoration, image denoising and artifacts removed in compressed images.

Youngjin Yoon et.al [20]. Introduced super resolution approach for light field (LF) images, these LF images will help in many diagnoses based applications. It is three step process to model SR problem with input LR images. these steps are to increase the spatial resolution with bicubic interpolation then applied to spatial SR network for enhancing the high frequency details and is given to angular network through which we can get three different views (horizontal,veritical and center) of the image. The proposed method also gets benefit by using single angular SR network instead of three in previous method, for three different input images. The advantage of this approach is limited training data set and minimum number of parameters is needed.

III. METHODOLOGY

Removal of noise in images, enhancing the quality of the frame, image restoration and processing speed are the main concerns in VLSI based image processing systems. Since raw input image acquires much noise, blurriness and poor contrast, hence it needs to be further processing. While considering medical images due to image acquisition and transmission they are often corrupted by impulse noise or speckle. Image processing circuits typically associated noise detector with this to reduce noise and enhance quality of the image. In our proposed methodology we have presented basic idea about VLSI based image processing systems methodologies for reducing impulse/speckle noises and image restoration. The main objective in designing VLSI architecture is, the design should only require low computational complexity, low hardware cost and its power consumption also be small. The proposed methodology contains four phase first is the noise detector to detect the noisy pixel or corrupted pixel in the image based on the intensity of the corrupted image. Second is the edge detection method, here the points at which image brightness changes sharply are typically organized into a set of curved line segments termed as edges and by identifying those edge pixels the edge can be preserved. Our third phase is the super resolution method (preferably deep learning algorithms) in which we can replace the corrupted or noisy pixel using interpolation (Sub pixel image interpolation) and anti-aliasing techniques. Finally our fourth phase will be full filled by implementing the whole process in Mat lab and is converted into Verilog HDL which can be implemented on FPGA through which VLSI architecture is to be design for multi-image applications.

IV. CONCLUSION

Numerous Researchers have been proposed different approaches and algorithms for enhancing the quality of the low resolution images. In this paper we discuss the VLSI based design methodologies for developing image processor chip. We also present methods and limitations of different papers on super resolution for development of High resolution pictures from set of low resolution pictures.VLSI based image processor can have different processing elements, each of these elements can be designing separately and implemented on FPGA to check the functionality of the design. Convolution networks, sparse coding and deep learning methods are more advanced real time methods.

V. FUTURE DIRECTIONS

From the last two decades many Researchers have been proposed diverse calculations for development of HR pictures from set of LR pictures or by utilizing some iterative remaking strategies on given LR pictures. This paper gives a portion of the soonest and most doable SR calculations and their restrictions and also gives a few headings to future specialist's effective development of Real world imaging applications. Color imaging frameworks is more noticeable zone .The issue connected with the shading pictures is to adjusting the attributes of both shading channel cluster and interjection approach amid recreation stage. Medical Practitioners not ready to recognize or analyze the patient wellbeing status because of low determination pictures got from low quality picture securing frameworks. Notwithstanding that, some clamor (salt and pepper or dot) is included amid procurement of picture. Consequently to take out commotion and upgrade the determination of the picture is likewise essential.

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